WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of memory cells, arranged in rows and columns, each for storing information;

a first refresh timer for issuing a first refresh request at a first period;

a first refresh address generation circuit for generating and outputting a first refresh address in accordance with said first refresh request;

a second refresh timer for issuing a second refresh request at a period shorter than the first period;

a second refresh address generation circuit for generating a second refresh address independently of the first refresh address; and

a plurality of row select circuits, provided corresponding to memory cell rows, each for driving a corresponding row to a selected state in accordance with a received address signal, each row select circuit driving an addressed row to a selected state in accordance with one of said first refresh address and said second refresh address, and a response relation to the first and second refresh addresses in each row select circuit being alternatively set.

2. The semiconductor memory device according to claim 1, further comprising:

a first address select circuit for selecting said first refresh address in accordance with said first refresh request, to supply a selected first refresh address to the row select circuits; and

a second address select circuit for selecting said second refresh address in accordance with said second refresh request, to supply a selected second refresh address to the row select circuits.

3. The semiconductor memory device according to claim 1, wherein each of said row select circuits includes a program circuit for

programming a refresh address designating a memory cell row to be refreshed.

4. The semiconductor memory device according to claim 3, wherein said program circuit validates one of said first refresh address and said second refresh address.

5. The semiconductor memory device according to claim 1, wherein said second refresh address generation circuit includes a count circuit performing a counting operation in accordance with said second refresh request, to generate said second refresh address.

6. The semiconductor memory device according to claim 1, wherein each of said row select circuits includes:

a first decode circuit for decoding said first refresh address signal;

a second decode circuit for decoding said second refresh address signal;

a row drive circuit for driving a corresponding memory cell row to a selected state in accordance with output signals of the first and second decode circuits; and

a program circuit for setting either one of said first and second decode circuits in an operable state.

7. The semiconductor memory device according to claim 1, wherein said first refresh address generation circuit includes an address count circuit performing a counting operation in accordance with said first refresh request to generate the first refresh address, and

said semiconductor memory device further comprises;

an address select circuit for selecting said first refresh address to supply, in place of an externally applied address signal, a selected first refresh address to the row select circuits in accordance with said first refresh request.

8. The semiconductor memory device according to claim 1, wherein said plurality of memory cells are divided into a plurality of memory blocks each including a plurality of memory cells arranged in rows and columns, and

the first and second refresh addresses each includes a block address designating a memory block.

9. The semiconductor memory device according to claim 1, further comprising:

a conflict avoiding circuit for preventing a conflict in issuance timing between the first and second refresh requests.

10. The semiconductor memory device according to claim 9, wherein said conflict avoiding circuit includes a delay circuit for delaying one of said first and second refresh requests by a prescribed time.